PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	OCuLink BP Type ECR
DATE:	May 19, 2017
AFFECTED DOCUMENT:	OCuLink Specification version 1.0
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Part I

1. Summary of the Functional Changes

The backplane type (BP Type) signal was incompletely specified in the original OCuLink 1.0 specification. Table 2-2 now includes a Type of logic used for this signal. A definition is provided for the logic levels of this signal.

2. Benefits as a Result of the Changes

Specifying the functionality of the BP Type sideband allows designs to interoperate. Add the ability for this signal to be used for vendor specific purposes after it initially determines the interface type.

3. Assessment of the Impact

Existing hardware designed to the previous specification may need to be modified to comply with these changes.

4. Analysis of the Hardware Implications

The behavior of the BP Type signal is changed from the previous specification. VSP lines that are recommended for use with REFCLK must be differentially coupled through the cable.

5. Analysis of the Software Implications

No impact on software.

6. Analysis of the C&I Test Implications

No impact on testing.

NOTE: This document complements the CPRSNT# ECR. Both documents are necessary to fully understand the proposed changes.

Part II

Detailed Description of the change

Change Sections 1.3, 2.3 and 2.4 as follows (see next page):

1.3 Terms and Acronyms

Terms and Acronyms not defined in this section may be found in the *PCI Express Base Specification*, the *PCI Express External Cabling Specification*, or the *PCI Express Card Electromechanical Specification*. Table 0-1 lists terms and acronyms specific to this specification.

Table 0-1. Terms and Acronyms

Terms/Acronyms	Definitions
Auxiliary signals	Signals that are not defined in the *PCI Express Base Specification,* but are necessary for certain desired functions or system implementation.
Backp ~~-P~~lane (BP) Type	A method to detect the end point interface type.
Cable port	The connectors and signals associated with a specific x4 physical interface.
Downstream Port	Ports facing away from the Root Complex. The Root Complex and switches have Downstream Ports.
Fixed	Used to describe the gender of the mating side of the connector that accepts its mate upon mating. This gender is frequently, but not always, associated with the common terminology "receptacle". The term "Fixed" is adopted from EIA standard terminology as the gender that most commonly exists on the Fixed end of a connection.
Free	Used to describe the gender of the mating side of the connector that penetrates its mate upon mating. This gender is frequently, but not always, associated with the common terminology "plug". The term "Free" is adopted from EIA standard terminology as the gender that most commonly exists on the Free end of a connection.
Full Crossover	A pinout that connects all A side contacts to all B side contacts enabling mass termination of the cable.
Lane	One PCI Express Lane contains a differential pair for Transmit and another differential pair for Receive. A xN Link is composed of N Lanes.
Link	A collection of one or more PCI Express Lanes, providing the communication path between an Upstream and Downstream Port.
OCuLink	A small form factor Optical or Copper x4 PCI Express cable Link, targeting mobile and systems with small faceplate areas, for both external and internal cabling.
Port aggregation	The ability to aggregate multiple connectors to provide an equivalently larger connector (e.g., the ability to aggregate two or four x4 connectors to construct x8 or x16 equivalent connectors).
Sideband signaling	A method for signaling Link events and conditions using physical signals that are separate from those signals which form the main data Link between two components.
Subsystem	In the context of this Specification, Subsystem is a generic term, identifying either an Upstream or Downstream device, providing a cabled PCI Express Port.
Upstream Port	Ports facing towards the Root Complex. Switches and End Points have Upstream Ports.
VSP	Vendor-specific Position.

2.3 Signal Description

Upstream/ Downstream port assignment is defined as shown in Figure 2-x below. This naming convention is consistent across all PCI Express documentation. Refer to the *PCI Express Base Specification* for more information.

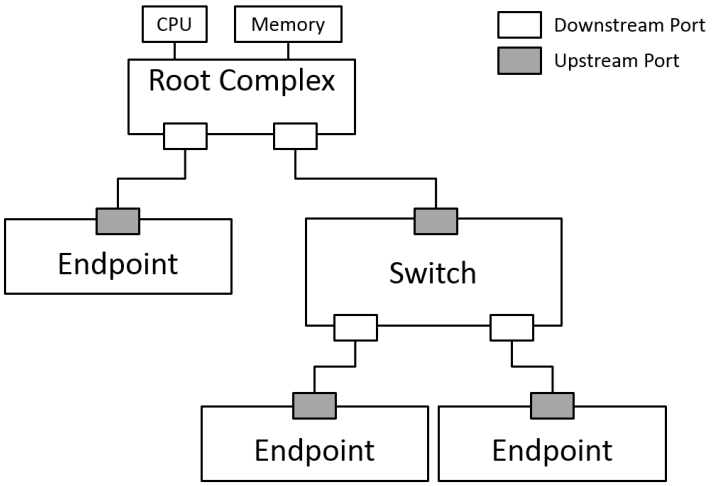

Figure 2-x. Upstream/ Downstream Port Assignment

Table ~~0~~2-2. Signal Description

Leave remaining content in this section as is.

2.4. Signal Compatibility Matrix

- All auxiliary signals are required from a cabling perspective.
- The signals listed in Table 2-2 are for an Upstream and/or Downstream Subsystem, with a brief description of features enabled by it.

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Table 2-2. Signal Compatibility Matrix

Signal	Type	~~Root/~~ Downstream ~~Subsystem~~Port (Note 1)	Cable Assembly	~~End Point/~~ Upstream ~~Subsystem~~Port (Note 1)	Comments
CPRSNT#	3.3 V Logic	Required Output	Connection Required	Required Input	Required on both sides of the cable. The driver is open-drain type and requires high impedance during power off states. Two possible states. Possible states: High (3.3V) and (3.3V)/2.
CWAKE#/ (OBFF) (Note 2)	3.3 V Logic	Optional Input/ (Optional I/O)	Connection Required	Optional Output/ (Optional I/O)	Optional on both sides of the cable. The driver is open-drain type and requires high impedance during power off states. If wake functionality is supported, this signal is input by the Downstream Port and output by the Upstream Port. If both ends support OBFF, the signal becomes bidirectional.~~Signal becomes bidirectional if both ends support OBFF.~~
PERST#	3.3 V Logic	Required Output	Connection Required	Required Input	When negated indicates that the applied main power is within the specified tolerance and is stable. A Downstream Subsystem must reset itself when this signal is asserted. ~~when the applied main power is within the specified tolerance and is stable. (Cable installed and power not applied).~~
VSP	User Defined	Optional I/O	Connection Required (Notes ~~1,2,~~3, 4, 5)	Optional I/O	Optional on both sides of the cable, function specified by vendor, is permitted to be used to support legacy functions or future functionality.
BP TYPE / (VSP) (Note 2)	3.3 V Logic	Optional Out~~In~~put/ (Optional I/O)	Connection Required (Note ~~6~~5)	Optional In~~Out~~put/ (Optional I/O)	Input required to enable a full crossover internal cable solution.

Notes:

1. Upstream Port and Downstream Port are defined in Table 1-1 and illustrated in Figure 2-x.
2. The first signal type listed is required to support OCuLink functionality; the associated Upstream Port/ Downstream Port assignments for this signal type are listed first in their respective columns. The second signal type, listed in parentheses, is an optional implementation; Upstream Port/ Downstream Port assignments associated with these options are also listed second, in parentheses, in their respective columns.
3. The SMBus/ 2-Wire interface employed in this specification can be a Passive or Active implementation. The Passive solution may provide a connection between Subsystems to: a) determine its usage or b) for device management. Due to complexity, Active Optical Cables may not want to implement this option and are permitted to have a reduced feature set. Requirements for PCI Express cables with reduced feature sets are described in SFF-8449.

1. Clocking architecture is beyond the scope of this specification; refer to Section 9.6 of the *PCI Express Base Specification* for more information. If The use of SMBus across the cable is an optional feature. This allows the use of cables that adhere to SFF-8449 for a PCI Express interface with a reduced feature set. Active Optical Cable assemblies may not want to implement SMBus across the cable for cost or complexity reasons, and therefore is permitted to have a reduced feature set. The Upstream Subsystems should not be designed in such a way as to require the use of SMBus across the cable. However, the SMBus controller is still required by both Upstream and Downstream fixed ends to read the cable assembly information for configuration of the PCIe devices that are part of the cabled Link.
2. 4. It is recommended that systems employing VSP is employed for common REFCLK, it is recommneded that systems utilize pins A12/A13 for REFCLK+/REFCLK- for Upstream Ports and pins B12/B13 for REFCLK+/ REFCLK- for Downstream Ports, and these connections must be differentially coupled. functionality utilize pins A12+/A13- for the ROOT and pins B12+/B13- for the ENDPOINT
3. SRIS architecture on Upstream and Downstream Subsystems is required if supporting no-wire VSP positions between Upstream and Downstream Subsystems
4. Verify systems enabling unshielded wire at VSP positions meet EMI emission and EMI susceptibility limits, as required by target market regulatory bodies.
5.
6. Refer to SFF-8448 for signaling details (Other 2-Wire Type). Once the Backplane Type has been determined, it does not preclude the Subsystem from using this signal for some other user/ vendor specific application.

Logic levels 0 and 1 are based on CMOS 3.3 V logic VIL≤0.3 × VCC, VIH≥0.7 × VCC. The high signaling level indicates 2-wire interface. A low signal level indictes SGPIO (refer to SFF-8448). The Endpoint must have a 4.7 kΩ resistor with a relative tolerance of 5% connected to VCC. Once the Backplane Type has been determined, it does not preclude the Controller/ Root from using this signal for some other user/vendor specific defined application.

Part III

Detailed Description of the chang

NOTE: *The changes included in this document dictate that changes must be made to the Wiring Chart ECR. These changes will be incorporated into the Wiring Chart ECR independently.*